

What is Claimed is:

- [c1] A digital Delay-Lock-Loop (DLL) circuit comprising:
 - a phase generator operable to produce a first clock signal having a first rising edge and a second clock signal having a second rising edge, wherein a timing difference between said first rising edge and said second rising edge is equal to a desired cycle time;
 - a delay circuit operable to receive said first clock signal and to produce a delayed clock signal; and
 - a latch element connected to said delay circuit, said latch element operable to check whether said delayed clock signal is delayed by an amount equal to said desired cycle time.
- [c2] The DLL circuit of claim 1, wherein said delay circuit comprises a plurality of binary-weighted inverters, said inverters operable to adjust a delay of said delayed clock signal to be equal to said desired cycle time.
- [c3] The DLL circuit of claim 1, further comprising a phase-shifted delay circuit connected to said delay circuit, said phase-shifted delay circuit operable to produce a phase shift of said delayed clock signal.
- [c4] The DLL circuit of claim 3, wherein said phase shift comprises multiple degrees of phase shift.
- [c5] The DLL circuit of claim 1, further comprising a filter connected to said latch element, said filter operable to send a final value of said delayed clock signal to said phase-shifted delay circuit.
- [c6] The DLL circuit of claim 5, further comprising a digital average function generator connected to said filter, wherein said digital average function generator is operable to instantaneously average previous comparisons of said delayed clock signal with said desired cycle time to produce said final value.
- [c7] The DLL circuit of claim 6, wherein said previous comparisons equal eight most recent previous comparisons.
- [c8] A digital Delay-Lock-Loop (DLL) circuit comprising:

a phase generator receiving a clock signal and outputting a first clock line and a second clock line, wherein a timing difference between said first clock line and said second clock line is equal to a desired cycle time; a first delay circuit receiving said first clock line and outputting a delayed clock signal; a second delay circuit receiving said delayed clock signal and producing a phase shift of said delayed clock signal; and a latch element operatively connected to said first delay circuit, wherein said latch element compares whether said delayed clock signal is delayed by an amount equal to said desired cycle time.

- [c9] The DLL circuit of claim 8, wherein said delay circuit comprises a plurality of serially connected binary-weighted delay elements, wherein said delay elements are operable to adjust a delay of said delayed clock signal to be equal to said desired cycle time.
- [c10] The DLL circuit of claim 8, wherein said phase shift comprises multiple degrees of phase shift.
- [c11] The DLL circuit of claim 8, further comprising a register connected to said latch element, said register operable to send a final value of said delayed clock signal to said phase-shifted delay circuit.
- [c12] The DLL circuit of claim 11, further comprising a digital average function generator connected to said register, wherein said digital average function generator is operable to instantaneously average previous comparisons of said delayed clock signal with said desired cycle time to produce said final value.
- [c13] The DLL circuit of claim 12, wherein said previous comparisons equal eight most recent previous comparisons.
- [c14] A method of producing a phase shift in a digital Delay-Lock-Loop (DLL) circuit, said method comprising:
 - generating a first clock signal having a first rising edge and a second clock signal having a second rising edge from a phase generator, wherein a timing difference between said first rising edge and said second rising

edge is equal to a desired cycle time; sending said first clock signal to a delay circuit; generating a delayed clock signal in said delay circuit; comparing a delay of said delayed clock signal with said desired cycle time in a latch element, wherein said delay circuit comprises said latch element; and generating a phase shift of said delayed clock signal in a phase-shifted delay circuit.

- [c15] The method of claim 14, further comprising adjusting said delay of said delayed clock signal to be equal to that of said desired cycle time, wherein said adjusting occurs in a plurality of binary-weighted inverters in said delay circuit.
- [c16] The method of claim 14, wherein said phase shift comprises multiple degrees of phase shift.
- [c17] The method of claim 14, further comprising transferring a final value of said delayed clock signal to said phase-shifted delay circuit, wherein said transferring is performed by a filter connected to said latch element.
- [c18] The method of claim 17, further comprising averaging previous comparisons of said delayed clock signal with said desired cycle time to produce said final value, wherein said averaging occurs in a digital average function generator connected to said filter.
- [c19] The method of claim 18, wherein said previous comparisons equal eight most recent previous comparisons.
- [c20] The method of claim 18, wherein said averaging occurs instantaneously.